This listing will replace all prior versions and listings of claims:

1-27. (Canceled)

28. (Currently amended) A method of processing a semiconductor wafer comprising:

(a) providing the wafer to an electrofill station in a module or cluster tool;

(b) in the electrofill station, electroplating copper on the wafer to fill high aspect ratio features;

(c) transferring the wafer to a second station in said module or cluster tool; ~~and~~

(d) in the second station, at least partially electromechanically polishing or electroplanarizing the wafer;

(e) transferring the wafer to another station in said module or cluster tool; and

(f) in the other station, wet etching the wafer.

29. (Previously presented) The method of claim 28, wherein the electrofill station employs an electrofill electrolyte and the second station employs a second electrolyte, and wherein the electrofill electrolyte and the second electrolyte have different compositions.

30. (Previously presented) The method of claim 28, wherein copper is electroplated on the wafer to at least partially fill low aspect ratio features not completely filled during electroplating in the electrofill station.

31. (Previously presented) The method of claim 30, wherein the copper is electroplated on the wafer to at least partially fill low aspect ratio features at a station other than the electrofill station.

32. (Previously presented) The method of claim 31, wherein the electrofill station includes an electrolyte comprising an additive.

33. (Previously presented) The method of claim 32, wherein the additive comprises a suppressor, an accelerator, or both.

34. (Previously presented) The method of claim 33, wherein the accelerator is selected from the group consisting of MPS, SPS, and DPS.

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35. (Previously presented) The method of claim 32, wherein the station in which copper is electroplated on the wafer to at least partially fill low aspect ratio features includes an electrolyte containing little or no additives.

36. (Previously presented) The method of claim 28, wherein the method is performed in an apparatus comprising separate modules for electroplating and polishing or planarization.

37 (Previously presented) The method of claim 28, wherein the electromechanically polishing or electroplanarizating is performed sequentially using a plurality of stations

38. (Previously presented) The method of claim 28, further comprising performing metal chemical etching on the semiconductor wafer.

39. (Cancelled)

40. (Currently amended) The method of claim 28, further comprising etching ~~on~~ the semiconductor wafer to remove copper from the wafer's edge bevel and/or backside region.

41. (Currently amended) A method of processing a semiconductor wafer comprising:

(a) providing the wafer to an electrofill station where copper is electroplated on the wafer to fill high aspect ratio features;

(b) providing the wafer to a second plating station where copper is electroplated on the wafer to cover low aspect ratio features not filled during electroplating in the electrofill station; ~~and~~

(c) electromechanically polishing or electroplanarizing the wafer sequentially using a plurality of stations,

wherein (a) – (c) are performed in an apparatus comprising separate modules for electroplating and planarization; and

(d) wet etching the wafer in another station.

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